IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A continuous-time operational amplifier comprising means for introducing an additional current to at least one internal node of said continuous-time operational amplifier for reducing an output offset voltage of said continuous-time operational amplifier, wherein said means for introducing include a voltage source connected between gates of two transistors.

2. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 1, wherein said means for introducing ~~an additional current~~ further comprise ~~a direct-current voltage source and~~ a transconductor, said ~~direct-current~~ voltage source applying a voltage to said transconductor and said transconductor providing said additional current.

3. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 2, wherein said voltage which is applied by said ~~direct-current~~ voltage source to said transconductor can be varied.

4. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 2, wherein said transconductor is realized as differential stage.

5. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 4, wherein said transconductor comprises a differential stage with a first, a second, a third and a fourth transistor, wherein said first and second transistors are said two transistors, each of said first, second, third and fourth transistor having a source, a gate and a drain, wherein a bias voltage is applied to said gates of said first and said second transistor, wherein said ~~direct-current~~ voltage source applies an additional voltage to said gate of said first transistor, wherein said sources of said first and said

second transistor are connected to a supply voltage of said operational amplifier, wherein said sources of said third and said fourth transistor are connected to ground, wherein said drains of said first and said second transistor are connected to said drains of said third and said fourth transistor, respectively, wherein said gate and said drain of said third transistor are short-circuited to each other, wherein said connection between said drains of said second and said fourth transistor are connected to an internal node of said operational amplifier for introducing ~~an~~ the additional current to said operational amplifier.

6. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 5, wherein ~~applying an~~ the additional voltage applied to said gate of said first transistor comprises ~~applying~~ a differential voltage signal applied to said gates of said first transistor and said second transistor.

7. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 1, further comprising feedback means for detecting an output offset voltage of said

operational amplifier and for controlling said means for introducing ~~an additional current~~ according to a detected offset.

8. (Currently Amended) ~~Operational~~ The continuous-time operational amplifier according to claim 1, further comprising for its normal operation a differential input stage and a second stage connected to each other, wherein said means for introducing ~~an additional current~~ apply said additional current to a node of said differential input stage.

9. (Currently Amended) ~~Operational~~ A continuous-time operational amplifier ~~according to claim 8,~~ comprising:

means for introducing an additional current to at least one internal node of said continuous-time operational amplifier for reducing an output offset voltage of said continuous-time operational amplifier; and

a differential input stage and a second stage connected to each other, said means for introducing applying said additional current to a node of said differential input stage, wherein said differential input stage comprises a first, a second, a third and a

fourth transistor, each of said first, second, third fourth transistor having a source, a gate and a drain, wherein said gates of said first and said second transistor are connected to different input terminals of said operational amplifier, wherein said sources of said first and said second transistor are connected to a supply voltage of said operational amplifier, wherein said sources of said third and said fourth transistor are connected to ground, wherein said drains of said first and said second transistor are connected to said drains of said third and said fourth transistor, respectively, wherein said gate and said drain of said third transistor are short-circuited to each other, wherein said connection between said drains of said second and said fourth transistor is connected to said second stage, and wherein said means for introducing an additional current apply said additional current to said connection between said drains of said first and said third transistor.

10. (Currently Amended) ~~Method~~ A method for reducing an output offset voltage of a continuous-time operational amplifier, said method comprising the acts of:

providing a voltage source between gates of two transistors; and

introducing an additional current using the voltage source to at least one internal node of said continuous-time operational amplifier.